ABSTRACT

The present invention is directed to a system and method of testing an integrated circuit (IC) device for potential latch-up. The system has a power supply configured to supply a maximum voltage to the integrated circuit device. The system uses a current measuring device for measuring current between the power supply and the circuit device. The system includes an overvoltage source that is operative to apply an overvoltage pulse to one input pin that is designated a test pin while the maximum supply voltage is applied to each other input pin of the integrated circuit device. The current measuring device detects whether a latch up condition exists by detecting an increase in current between the power supply and the device based application of the overvoltage pulse.